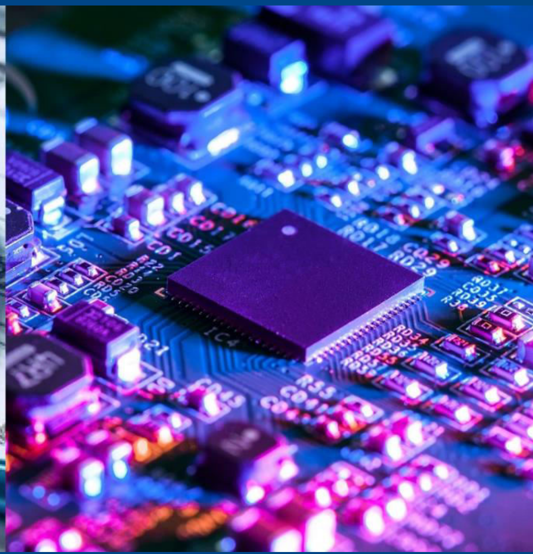
ISSN: 2582-7219

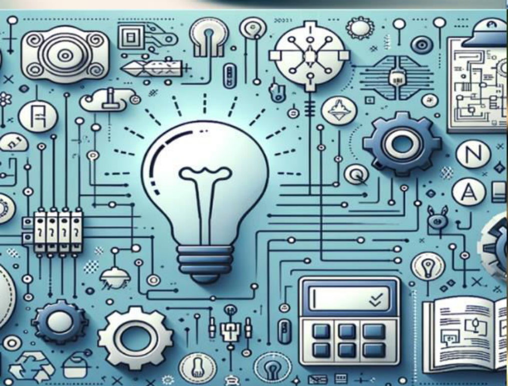




International Journal of Multidisciplinary Research in Science, Engineering and Technology

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)



Impact Factor: 8.206

Volume 9, Issue 3, March 2026

www.ijmrset.com ijmrset@gmail.com +91 6381 907 438 +91 63819 07438

ISSN: 2582-7219 | www.ijmrset.com | Impact Factor: 8.206| ESTD Year: 2018|

International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

Low Power MAC Architecture used in DSP Applications

G.Jahnavi[1], B.Pavani[2], .CH.N.Mukesh[3], K.S.R.Tagore[4], L.J.N.Sree Lakshmi[5]

U.G. Students, Department of ECE, SVIET Engineering College, Nandamuru, Pedana, Andhra Pradesh, India[1-4]

Assistant Professor, Department of ECE, SVIET Engineering College, Nandamuru, Pedana, Andhra Pradesh, India[5]

ABSTRACT: Multiply–Accumulate (MAC) units are fundamental building blocks in Digital Signal Processing (DSP) systems such as filters, image processing, and communication applications. The performance of DSP systems highly depends on the efficiency of the MAC unit in terms of speed, power consumption, and area. In this work, a low-power and high-speed MAC architecture is proposed using an optimized 4:2 compressor for efficient partial product reduction. The proposed design integrates a compressor-based multiplier with a Carry Lookahead Adder (CLA) for fast accumulation. Additionally, a Baugh–Wooley multiplication technique is incorporated to support signed arithmetic operations with reduced latency. The architecture is implemented using hardware description language and evaluated through simulation. Experimental results demonstrate that the proposed MAC unit achieves reduced propagation delay, lower power consumption, and improved performance compared to conventional MAC designs, making it suitable for modern DSP applications.

KEYWORDS: MAC Unit, DSP, 4:2 Compressor, Baugh-Wooley Multiplier, Low Power Design, Carry Lookahead Adder, FPGA, VLSI

I. INTRODUCTION

Digital Signal Processing systems are widely used in communication, audio processing, video processing, image processing, biomedical systems, and embedded applications. DSP operations mainly involve multiplication and addition operations, which are performed by Multiply-Accumulate (MAC) units. A MAC unit performs multiplication of two input numbers and adds the result to the previous accumulated value. Since MAC operations are repeatedly used in DSP algorithms such as FIR filters, FFT, and convolution operations, the efficiency of MAC architecture is very important.In conventional MAC architectures, multiplication is performed using array multipliers or Wallace tree multipliers, and accumulation is performed using ripple carry adders. These architectures suffer from high delay and power consumption due to long carry propagation paths and multiple addition stages.

To overcome these problems, compressor circuits are used in multiplier architecture to reduce the number of partial product reduction stages. The 4:2 compressor reduces four input bits into two output bits, which reduces hardware complexity and delay. Carry Lookahead Adders are used to improve the speed of the accumulation stage.This paper proposes a low-power MAC architecture using a compressor-based multiplier and carry lookahead accumulator to improve speed and reduce power consumption.

II. RELATED WORK

Several multiplier architectures have been proposed in the literature to improve speed and reduce power consumption. Shift-and-add multipliers are simple but slow due to sequential operations. Wallace tree multipliers reduce delay by using parallel addition but require more hardware. Booth multipliers reduce the number of partial products but require complex encoding logic. Dadda multipliers reduce hardware usage compared to Wallace multipliers but still involve multiple addition stages.

Recent research focuses on compressor-based multipliers where compressors replace full adders in the partial product reduction stage. Compressors reduce the number of addition stages, thereby reducing delay and power consumption.

Carry Lookahead Adders are commonly used in accumulator stages because they reduce carry propagation delay

ISSN: 2582-7219 | www.ijmrset.com | Impact Factor: 8.206| ESTD Year: 2018|

International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

compared to ripple carry adders .However, many existing MAC architectures treat multiplier and accumulator separately, which increases delay. The proposed architecture integrates compressor multiplier and accumulator efficiently to improve performance.

III. METHODOLOGY

The proposed MAC architecture is built around three major stages: partial-product generation, partial-product compression, and accumulation. The Baugh–Wooley algorithm is adopted to handle two's-complement signed multiplication while preserving a regular array structure, which simplifies mapping to hardware. Once the partial products are generated, a network of 4:2 compressors, along with a few required full adders and half adders, is used to compress the multi-row matrix into only two rows. These final two rows are summed by a CLA adder, and the result is accumulated with the previous MAC output stored in a register, completing the MAC operation. The entire architecture is modeled at RTL level, enabling easy synthesis and verification using standard digital design tools. The MAC architecture consists of Four main stages:

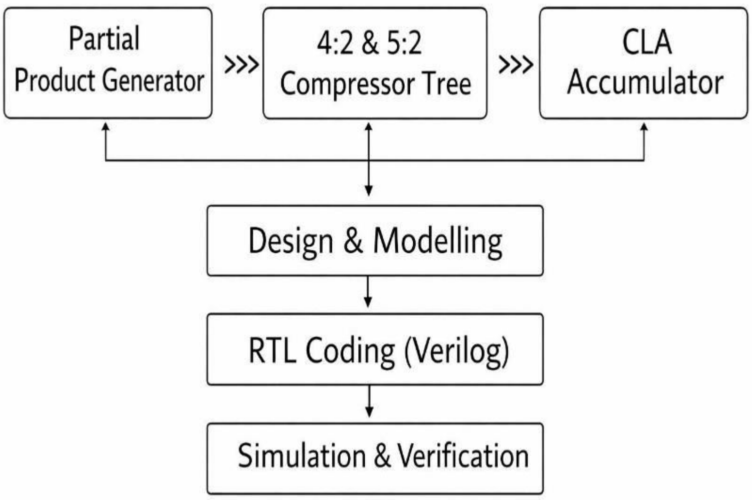


Fig A: Proposed Methodology

1. Partial Product Generation: The partial products are generated by using AND gates between the multiplier and multiplicand bits.
2. Compressor Based Reduction Unit: The partial products are generated by partial product generator is reduced by using a 4:2 compressor tree. The compressor is used to reduce multiple input bits into sum and carry outputs.
3. Final Adder: The reduced outputs are added by using a carry lookahead adder to generate the final multiplication result.
4. Accumulator: The multiplication results generated by final adder by using carry lookahead adder is added to the previous accumulated value and the output is stored in a register.

Parameters	Conventional MAC	Proposed MAC
Delay	High	Low
Power	High	Reduced
Area	Large	Optimized
Speed	Moderate	High

Table 1: Comparison between Conventional MAC and Proposed MAC

ISSN: 2582-7219 | www.ijmrset.com | Impact Factor: 8.206| ESTD Year: 2018|

International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

IV. EXPERIMENTAL RESULTS

The proposed MAC architecture was simulated and verified using standard EDA tools. The results were analysed in terms of delay, power consumption, and functional correctness. The waveform analysis confirms correct multiplication and accumulation operations. The use of 4:2 compressors reduces the number of logic levels, resulting in lower propagation delay. Power consumption is reduced due to minimized switching activity and optimized logic design. The Carry Lookahead Adder improves the speed of accumulation compared to conventional adders. Comparative analysis shows that the proposed design outperforms traditional MAC architectures such as Wallace Tree and shift-and-add multipliers in terms of speed and power efficiency.

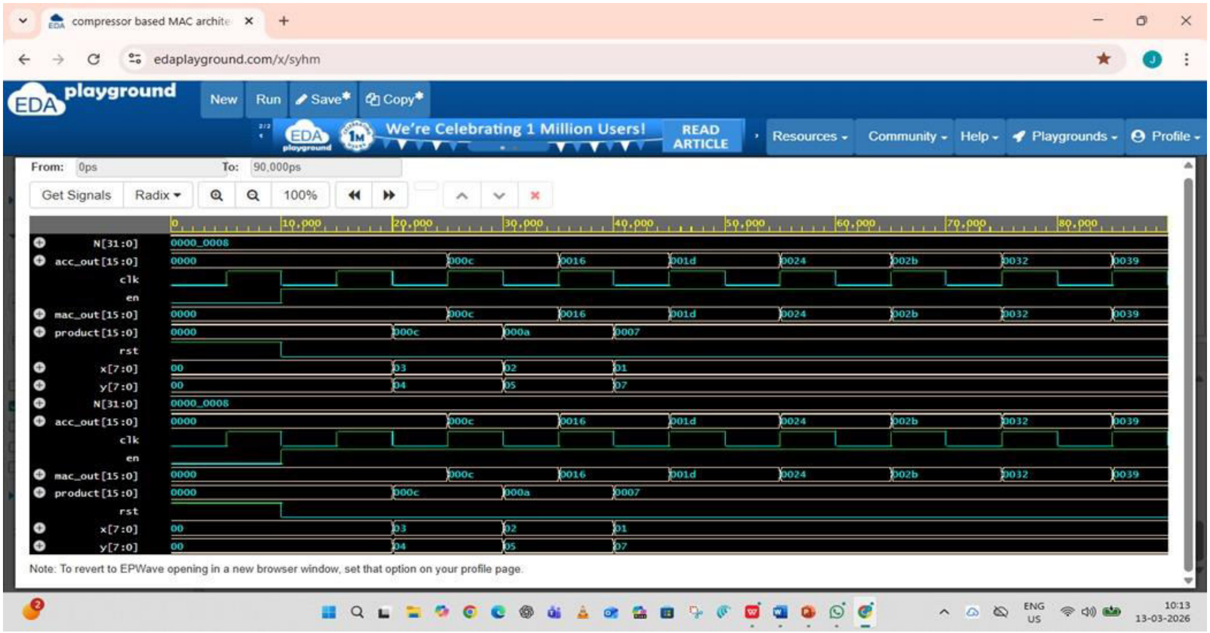


Fig B: Simulation results of the Final Accumulator

V. CONCLUSION

This paper presented a low-power and high-speed MAC architecture using a compressor-based multiplier and carry lookahead accumulator. The compressor reduces partial product reduction stages, which reduces delay and power consumption. The proposed MAC architecture improves speed and performance compared to conventional architectures. The design is suitable for DSP, image processing, and communication applications. Future work includes FPGA implementation and ASIC design.

REFERENCES

[1] Chang, Chip-Hong, JiangminGu, and Mingyan Zhang. "Ultra low-voltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits." Circuits and Systems I: Regular Papers, IEEE Transactions on 51.10 (2004): 1985-1997.

[2] Tung Thanh Hoang; Sjalander, M.; Larsson-Edefors, P., "A High-Speed, Energy Efficient Two-Cycle MultiplyAccumulate (MAC) Architecture and Its Application to a Double-Throughput MAC Unit," Circuits and Systems I: Regular Papers, IEEE Transactions on , vol.57, no.12, pp.3073,3081, Dec. 2010.

[3] Chen Ping-hua; Zhao Juan, "High-speed Parallel 32×32-b Multiplier Using a Radix-16 Booth Encoder," Intelligent Information Technology Application Workshops, 2009. IITAW '09. Third International Symposium on , vol., no., pp.406,409, 2122 Nov. 2009.

[4] Kiwon Choi; Minkyu Song, "Design of a high performance 32×32-bit multiplier with a novel sign select Booth encoder," Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on , vol.2, no.,

ISSN: 2582-7219 | www.ijmrset.com | Impact Factor: 8.206| ESTD Year: 2018|

International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

pp.701,704 vol. 2, 6-9 May 2001.
[5] Rajput, R.P.; Swamy, M.N.S., "High Speed Modified Booth Encoder Multiplier for Signed and Unsigned Numbers," Computer Modelling and Simulation (UKSim), 2012 UKSim 14th International Conference on , vol., no., pp.649,654, 28-30 March 2012.
[6] Yangbo Wu; Weijiang Zhang; Jianping Hu, "Adiabatic 4-2 compressors for low-power multiplier," Circuits and Systems, 2005. 48th Midwest Symposium on , vol., no., pp.1473,1476 Vol. 2, 7-10 Aug. 2005.
[7] Jaina, D.; Sethi, K.; Panda, R., "Vedic Mathematics Based Multiply Accumulate Unit," Computational Intelligence and Communication Networks (CICN), 2011 International Conference on, vol., no., pp.754,757, 7-9 Oct. 2011.
[8] Aliparast, Peiman, Ziaadin D. Koozehkanani, and FarhadNazari. "An Ultra High Speed Digital 4-2 Compressor in 65-nm CMOS."International Journal of Computer Theory & Engineering 5.4 (2013).
[9] N. Weste and David Harris, “CMOS VLSI Design- A Circuits & System Perspective”, Pearson Education, 2008.

INTERNATIONAL JOURNAL OF MULTIDISCIPLINARY RESEARCH IN SCIENCE, ENGINEERING AND TECHNOLOGY

| Mobile No: +91-6381907438 | Whatsapp: +91-6381907438 | ijmrset@gmail.com |

www.ijmrset.com